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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,890	03/12/2004	Andrew Burdass	550-530	4902

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EXAMINER	
JOHNSON, BRIAN P	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,890	BURDASS, ANDREW	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-30 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on March 12th, 2004. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 9-13, 16-21, and 24-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen (U.S. Patent No. 5,481,685).

5. Regarding claims 1 and 16, Nguyen discloses apparatus for processing data (col 3 line 42), said apparatus comprising: an instruction pipeline operable to hold a plurality of program instructions (col 14 lines 62-64) at respective different stages of instruction processing (col 26 lines 6-9), an execution stage of said instruction pipeline serving to execute a current program instruction held at said execution stage (col 26 lines 8-9); an

instruction prefetch unit operable to fetch program instructions from a memory system to said instruction pipeline (col 12 lines 47-52); and an exception controller responsive to an exception signal to trigger exception processing by forcing program execution starting from an exception handling program instruction (col 12 line 51) stored at a predetermined memory location (col 12 lines 54-56); wherein upon receipt of said exception signal part way through execution of said current program instruction (col 14 line 62 to col 15 line 4), said exception controller is operable to trigger said instruction prefetch controller to start fetching of said exception handling program instruction from said memory system prior to completion of execution of said current program instruction (col 12 lines 47-52).

6. Regarding claims 2 and 17, Nguyen discloses apparatus as in claim 1, wherein execution of said current instruction lasts for a plurality of clock cycles (col 26 lines 6-9)

Note that the different stages suggest different clock cycles.

And fetching of said exception handling program instruction starts part way through said plurality of clock cycles (col 12 lines 47-52).

Note that the effect of an exception is a "prefetch". The fetching occurs at least one clock cycle afterwards, making the actual fetching of the exception handler part way through the plurality of clock cycles.

7. Regarding claims 3 and 18, Nguyen discloses apparatus as in claim 1, wherein said exception handling program instruction redirects program execution to an exception handling routine (col 12 lines 47-52).

8. Regarding claims 4 and 19, Nguyen discloses apparatus as in claim 1, wherein said memory system comprises a cache memory and a main memory, said prefetch controller triggering a cache line fill operation upon a miss of a lookup for said exception handling program instruction within said cache memory (col 9 lines 13-18 and col 12 lines 47-52).

Note: see claim 9.

9. Regarding claims 5 and 20, Nguyen discloses apparatus as in claim 1, wherein said exception controller is an interrupt controller, said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction (col 25 lines 55-56).

10. Regarding claims 6 and 21, Nguyen discloses apparatus as in claim 1, wherein said exception is one of a data abort (col 14 line 62 to col 15 line 4)

Note that the data is aborted during the exception.

And a prefetch abort (col 27 lines 2-5).

Note that the prefetching is aborted during the exception.

11. Regarding claims 9 an d 24, Nguyen discloses apparatus for processing data, said apparatus comprising: a cache memory operable to store program instructions to be executed (fig 1 reference 132); and an exception controller responsive to an exception signal to trigger exception processing by forcing program execution starting from an exception handling program instruction stored at a predetermined memory location (col 12 lines 47-52); wherein upon receipt of said exception signal part way through execution of a current program instruction (col 14 line 62 to col 15 line 4), said exception controller is operable to trigger a lookup of said exception handling program instruction within said cache memory and if said exception handling program instruction is not present within said cache memory to trigger a cache linefill operation to read said exception handing program instruction from a main memory to said cache memory (col 9 lines 13-18).

Note that the reference explicitely states that during an exception/interrupt, the ISR routine is prefetched (col 12 lines 47-52). The reference does not explicitely state that the instruction cache will be checked before prefetching these instructions; however, this fact is clearly implied by the cited disclosure. One of skill in the art, who has even a vague understanding of memory hierarchy, would have realized that a cache is checked initially, then if a miss occurs, main memory is checked.

12. Regarding claims 10 and 25, Nguyen discloses apparatus as in claim 9, wherein execution of said current instruction lasts for a plurality of clock cycles (col 26 lines 6-9)

and lookup of said exception handling program instruction within said cache memory starts part way through said plurality of clock cycles (col 12 lines 47-52).

Note: see claim 2.

13. Regarding claims 11 and 26, Nguyen discloses apparatus as in claim 9, wherein said exception handling program instruction redirects program execution to an exception handling routine (col 12 lines 47-52).

14. Regarding claims 12 and 27, Nguyen discloses apparatus as in claim 9, wherein said exception controller is an interrupt controller, said exception signal is an interrupt signal and said exception handling program instruction is and interrupt handling program instruction (col 25 lines 55-56).

15. Regarding claims 13 and 28, Nguyen discloses apparatus as in claim 9, wherein said exception is one of a data abort (col 14 line 62 to col 15 line 4) and a prefetch abort (col 27 lines 2-5).

Note: see claim 6.

Claim Rejections - 35 USC § 103

16. Claims 7, 8, 14, 15, 22, 23, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen in view of Glass (U.S. Patent No. 5,784,602).

Regarding claims 7, 8, 14, 15, 22, 23, 29 and 30, Nguyen discloses the limitations on which these claims are dependant.

Nguyen fails to disclose a common core for processor components or, more generally, an integrated circuit.

Glass discloses a system on an integrated circuit (col 4 lines 21-25).

At the time of the invention, one skilled in the art would have been motivation to make the combination based on the reasoning disclosed in Glass that an integrated circuit "is highly advantageous for space, speed, power consumption and cost reasons" (col 4 lines 23-25).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Nguyen and implement it on a single integrated core, as in Glass.

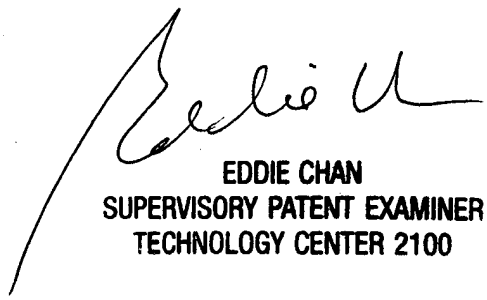
Conclusion

17. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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